REPLACEMENT SHEET

ATTY DKT. NO.: U.S. SERIAL NO.: 10/720,730 NOVEMBER 24, 2

INVENTOR(S):

CONF. NO.: 2757

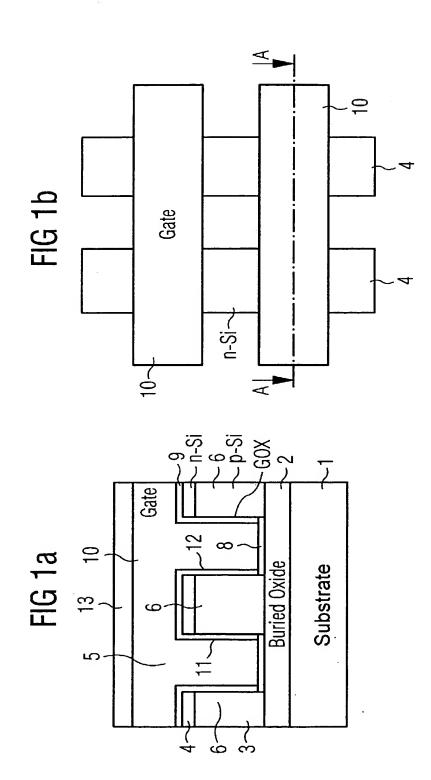
TITLE:

NOVEMBER 24, 2003
DRAM CELL ARRANGEMENT WITH VERTICAL MOS
TRANSISTORS, AND METHOD FOR ITS FABRICATION
TILL SCHLÖSSER ET AL.
SHEET 1 OF:

SHEET 1 OF 3



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REPLACEMENT SHEET

ATTY DKT. NO.: U.S. SERIAL NO.: FILED: TITLE:

INFN/WB0037 10/720,730

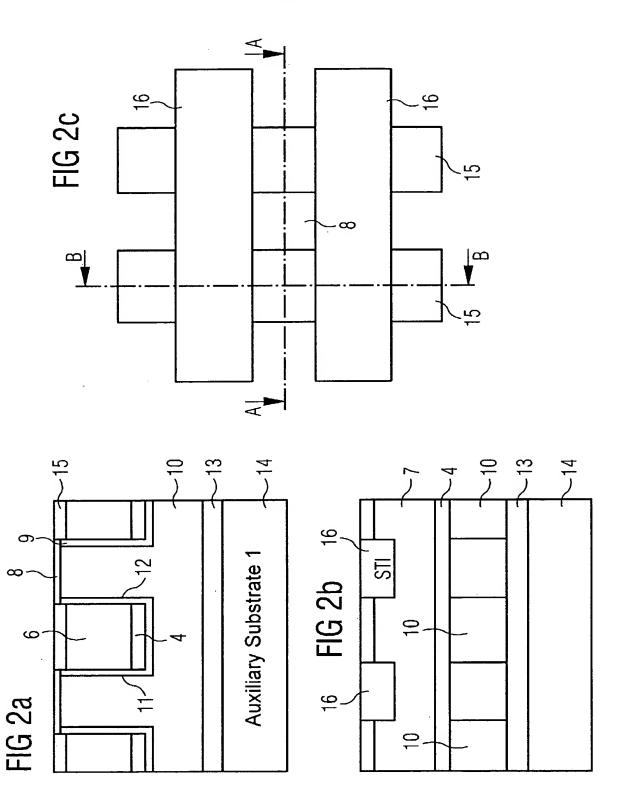
CONF. NO.: 2757

NOVEMBER 24, 2003
DRAM CELL ARRANGEMENT WITH VERTICAL MOS
TRANSISTORS, AND METHOD FOR ITS FABRICATION TILL SCHLÖSSER ET AL.

INVENTOR(S):

SHEET 2 OF 3

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REPLACEMENT SHEET

ATTY DKT. NO.: U.S. SERIAL NO.: FILED: TITLE:

INFN/WB0037
10/720,730 CONF. NO.: 2757
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TRANSISTORS, AND METHOD FOR ITS FABRICATION
THE SCHLÖSSER ET AL. SHEET 3 OF 3

INVENTOR(S):

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